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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/575,055	05/19/2000	Q.Z. Liu	99CON114P	2945

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EXAMINER

LUU, CHUONG A

ART UNIT PAPER NUMBER

2825

DATE MAILED: 12/19/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/575,055

Applicant(s)

LIU ET AL.

Examiner

Chuong A Luu

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 October 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The Rejections

Claims 1-2 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koo et al. (U.S. 5,677,234) in view of Chang et al. (U.S. 5,834,351)

Koo discloses a method of forming isolated semiconductor device active regions with

- (1) exposing a second area in said dielectric to a dielectric conversion source so as to increase said first dielectric constant of said dielectric in said second area to a second dielectric constant (see column 3, lines 12-35);
- (2) wherein said covering said dielectric with photoresist (see column 3, lines 12-35);

(6) wherein said dielectric conversion source comprises oxygen plasma (see column 3, lines 12-35) .

Koo teaches the above outlined features except for specific step of covering a first area in a dielectric, said dielectric having a first dielectric constant. However, Chang discloses a process for fabricating an integrated circuit device with **(1)**..... covering a first area in a dielectric, said dielectric having a first dielectric constant (see column 4, lines 57-58. Figure 1D). It would have been obvious to an ordinary skill in the art at the time of the invention was made to combine the teachings of Koo and Chang to manufacture a semiconductor device to exceed its performance criteria.

Claims 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koo et al. (U.S. 5,677,234) in view of Chang et al. (U.S. 5,834,351) and further in view of Gore et al. (U.S. 6,391,932 B1)

Koo and Chang disclose everything above except for wherein said dielectric conversion source comprises E-beams, I-beams and an amine based chemical. However, Hakey discloses integrated circuit chip produced by using frequency doubling hybrid photoresist with **(3)** wherein said dielectric conversion source comprises E-beams; **(4)** wherein said dielectric conversion source comprises I-beams; **(5)** wherein said dielectric conversion source comprises an amine based chemical (see columns 15 and 18, lines 13-30 and lines 32-48, respectively). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to

combine the above references to produce a semiconductor device to exceed its performance requirements by applying specific beams or chemical solution.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Koo et al. (U.S. 5,677,234) in view of Chang et al. (U.S. 5,834,351) and further in view of Hintermaier et al. (U.S. 6,303,391 B1)

Koo and Chang disclose everything above except for wherein said dielectric is hydrogen silsesquioxane. However, Hintermaier discloses a method of forming ferroelectric memory devices by (7) wherein said dielectric is hydrogen silsesquioxane (see column 9, lines 35-52). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above references to produce a semiconductor device to meet specific performance criteria.

Claims 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koo et al. (U.S. 5,677,234) in view of Chang et al. (U.S. 5,834,351) and further in view of Yu et al. (U.S. 6,372,632)

Koo and Chang disclose everything above except for etching a plurality of interconnect trenches in said first area in said dielectric and etching a plurality of capacitor trenches in said second area in said dielectric, filling each of said plurality of capacitor trenches and each of said plurality of interconnect trenches with metal, and metal is copper. However, Yu discloses a process of forming a planarized metal interconnect by (8) further comprising steps of: etching a plurality of interconnect

trenches in said first area in said dielectric and etching a plurality of capacitor trenches in said second area in said dielectric; **(9)** further comprising a step of filling each of said plurality of capacitor trenches and each of said plurality of interconnect trenches with metal; **(10)** wherein said metal is copper (see column 3, lines 12-32. Figure 1). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above references to produce a semiconductor device to exceed performance criteria.

Claims 11-17, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koo et al. (U.S. 5,677,234) in view of Chang et al. (U.S. 5,834,351) and further in view of Greco et al. (U.S. 5,925,960)

Koo discloses a method of forming isolated semiconductor device active regions with **(11)** exposing a second area in said dielectric to a dielectric conversion source so as to increase said first dielectric constant of said dielectric in said second area to a second dielectric constant (see column 3, lines 12-35).

Koo teaches the above outlined features except for specific step of covering a first area in a dielectric, a chemical mechanical, etching a plurality of interconnect trenches in a first area in said dielectric layer; etching a plurality of capacitor trenches in a second area in said dielectric layer; filling said plurality of interconnect trenches and said plurality of capacitor trenches with metal; performing a chemical mechanical polish on said first and second areas; exposing said second area in said dielectric layer to a dielectric conversion source so as to increase said first

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dielectric constant of said dielectric layer in said second area to a second dielectric constant; wherein said metal is copper. However, Chang discloses a process for fabricating an integrated circuit device with **(11)**..... covering a first area in a dielectric, said dielectric having a first dielectric constant (see column 4, lines 57-58. Figure 1D). Furthermore, Greco discloses a process for reducing pattern factor effects in CMP planarization by **(11)**..... etching a plurality of interconnect trenches in said first area in said dielectric layer; etching a plurality of capacitor trenches in said second area in said dielectric layer; filling said plurality of interconnect trenches and said plurality of capacitor trenches with metal; **(12)** further comprising a step of performing a chemical mechanical polish after said filling step; **(13)** wherein said metal is copper; **(14)** forming a dielectric layer in a semiconductor die, said dielectric layer having a first dielectric constant; etching a plurality of interconnect trenches in a first area in said dielectric layer; etching a plurality of capacitor trenches in a second area in said dielectric layer; filling said plurality of interconnect trenches and said plurality of capacitor trenches with metal; performing a chemical mechanical polish on said first and second areas; exposing said second area in said dielectric layer to a dielectric conversion source so as to increase said first dielectric constant of said dielectric layer in said second area to a second dielectric constant; **(15)** wherein said metal is copper; **(16)** depositing a metal layer in a semiconductor die; etching said metal layer to form a plurality of interconnect lines in a first area of said semiconductor die and a plurality of capacitor electrodes in a second area of said semiconductor die; depositing a gap fill dielectric between said plurality of capacitor electrodes and between said plurality of interconnect lines;

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covering said first area in said gap fill dielectric, said gap fill dielectric having a first dielectric constant; exposing said second area in said gap fill dielectric to a dielectric conversion source so as to increase said first dielectric constant of said gap fill dielectric in said second area to a second dielectric constant; **(17)** wherein said covering step comprises covering said first area in said gap fill dielectric with photoresist; **(23)** wherein said metal layer comprises aluminum (see columns 9 and 10, lines 4-67 and lines 1-4, respectively. Figures 7-9). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above references to produce a semiconductor device to meet specific criteria performance.

Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koo et al. (U.S. 5,677,234) in view of Chang et al. (U.S. 5,834,351) and Greco et al. (U.S. 5,925,960) and further view of Hakey et al. (U.S. 6,313,492 B1)

Koo, Chang and Greco teach everything above except for wherein said dielectric conversion source comprises E-beams, I-beams and an amine based chemical. However, Hakey discloses integrated circuit chip produced by using frequency doubling hybrid photoresist by **(18)** wherein said dielectric conversion source comprises E-beams (see column 1, lines 38-39); **(19)** wherein said dielectric conversion source comprises I-beams (see column 1, lines 35-40); **(20)** wherein said dielectric conversion source comprises an amine based chemical (see column 9, lines 44-54). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to

combine the above references to produce a semiconductor device to meet specific criteria performance.

Claims 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koo et al. (U.S. 5,677,234) in view of Chang et al. (U.S. 5,834,351) and Greco et al. (U.S. 5,925,960) and further view of Hintermaier et al. (U.S. 6,303,391 B1)

Koo, Chang and Greco teach everything above except for wherein said dielectric conversion source comprises oxygen plasma and wherein said dielectric is hydrogen silsesquioxane. However, Hintermaier discloses a method of forming ferroelectric memory devices by **(21)** wherein said dielectric conversion source comprises oxygen plasma (see column 12, lines 31-46); **(22)** wherein said dielectric is hydrogen silsesquioxane (see column 9, lines 35-52). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the above references to produce a semiconductor device to meet specific criteria performance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A Luu whose telephone number is (703)305-0129. The examiner can normally be reached on M-F (7:30-4:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (703)308-1323. The fax phone numbers

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for the organization where this application or proceeding is assigned are (703)872-9318 for regular communications and (703)872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

CAL

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December 16, 2002

C. J. Jankowski
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